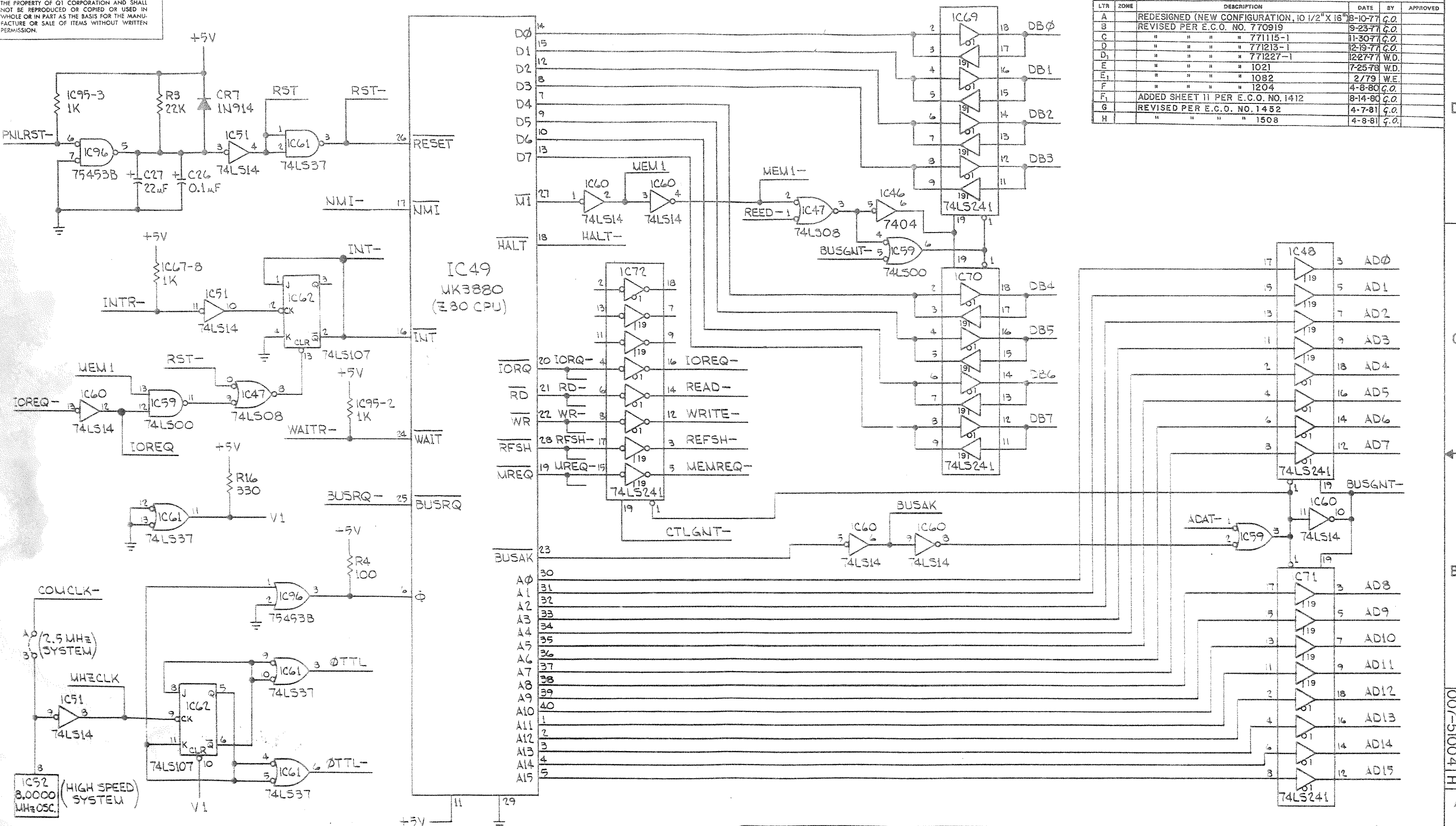


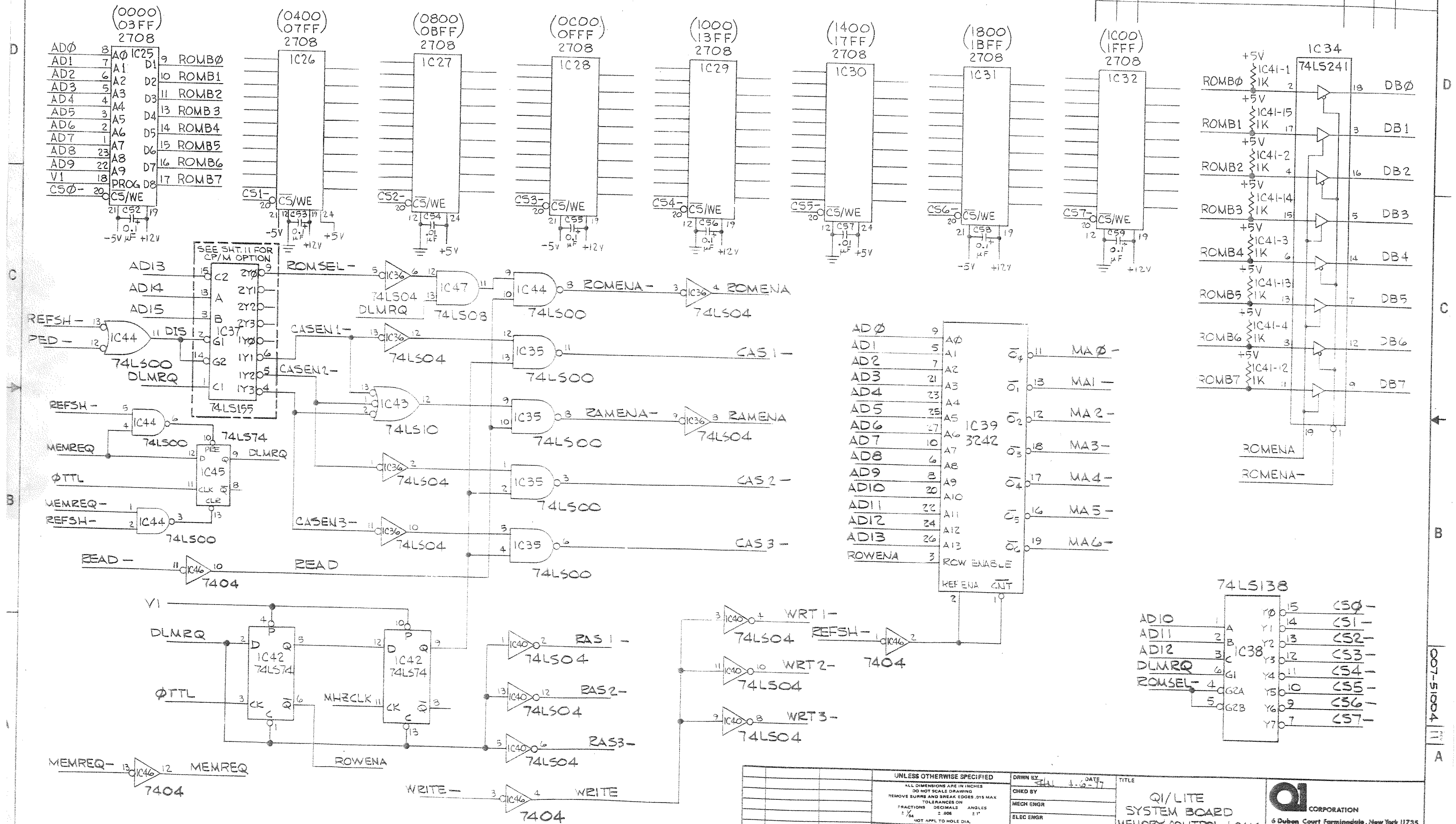
THIS DRAWING AND SPECIFICATIONS HEREIN ARE THE PROPERTY OF Q1 CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.



REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	BY
A		REDESIGNED (NEW CONFIGURATION, 10 1/2" X 16")	8-10-77	G.O.
B		REVISED PER E.C.O. NO. 770919	9-23-77	G.O.
C		" " " " 771115-1	11-30-77	G.O.
D		" " " " 771213-1	12-19-77	G.O.
D1		" " " " 771227-1	12-27-77	W.D.
E		" " " " 1021	7-25-78	W.D.
E1		" " " " 1082	2/79	W.E.
F		" " " " 1204	4-8-80	G.O.
F1		ADDED SHEET 11 PER E.C.O. NO. 1412	8-14-80	G.O.
G		REVISED PER E.C.O. NO. 1452	4-7-81	G.O.
H		" " " " 1508	4-8-81	G.O.

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING REMOVE BURRS AND BREAK EDGES TO MAX TOLERANCES ON FRACTIONS DECIMALS ANGLES ± 1/64 ± 0.005 ± 1°			OWN BY G.O'GRADY DATE 10-13-80	TITLE SCHEMATIC Q1/LITE SYSTEM BOARD CPU LOGIC	Q1 CORPORATION 125 Ricefield La. Hempstead New York 11787 SIZE DWG. NO. 007-51004 REV H D 007-51004 H SCALE SHEET 1 OF 11
DASH	NEXT ASSY	USED ON	APPROVED	SEE SEPARATE SHEET FOR LIST OF MATERIALS	
APPLICATION			RELEASE		

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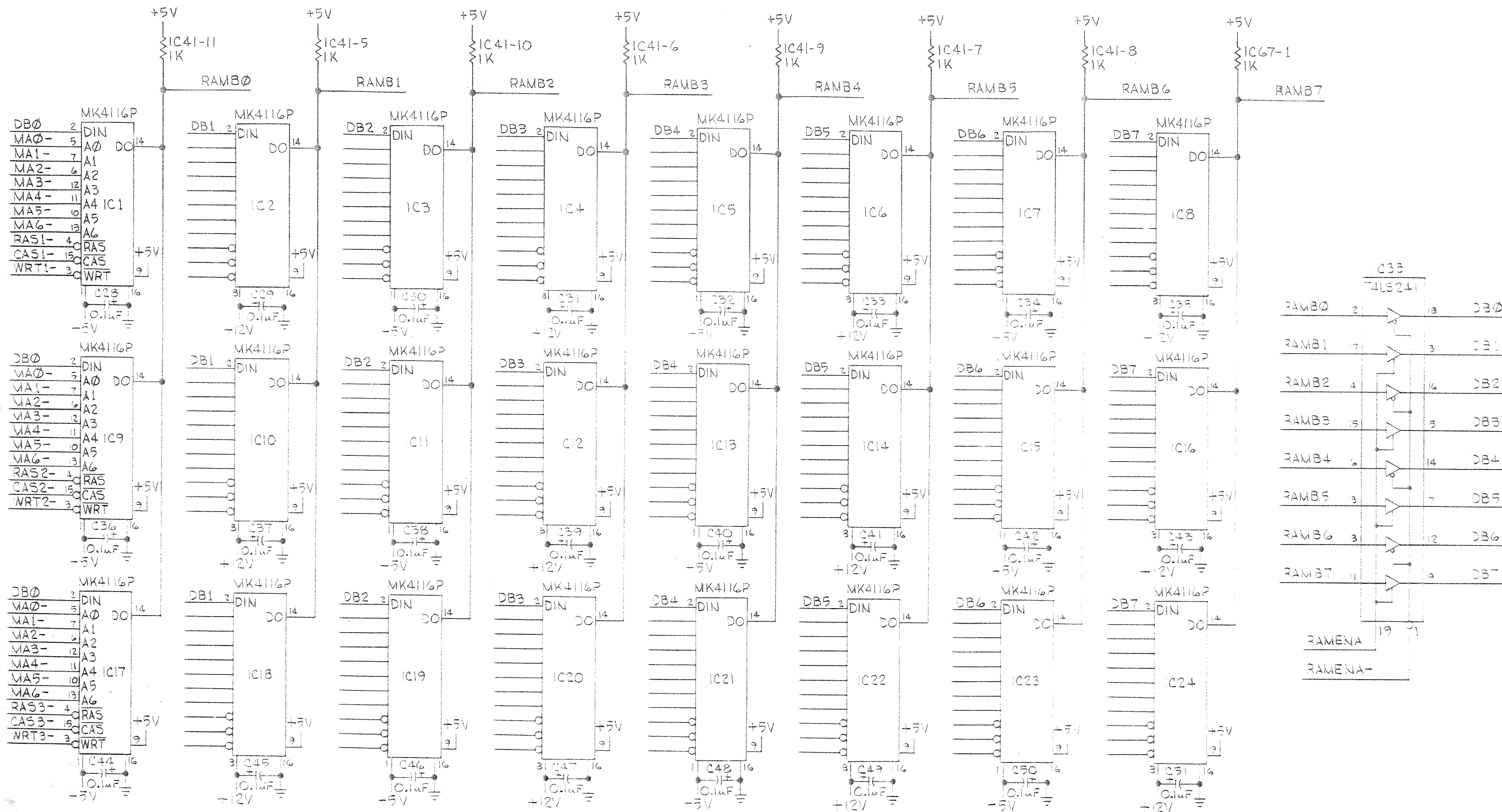



007-51004

100

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REVISIONS					
LTR	ZONE	DESCRIPTION	DATE	BY	APPROVED
		SEE SHT. - 1			

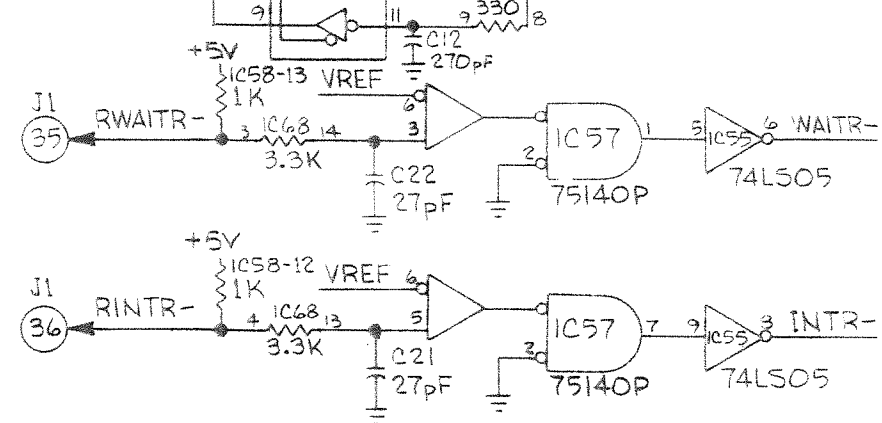
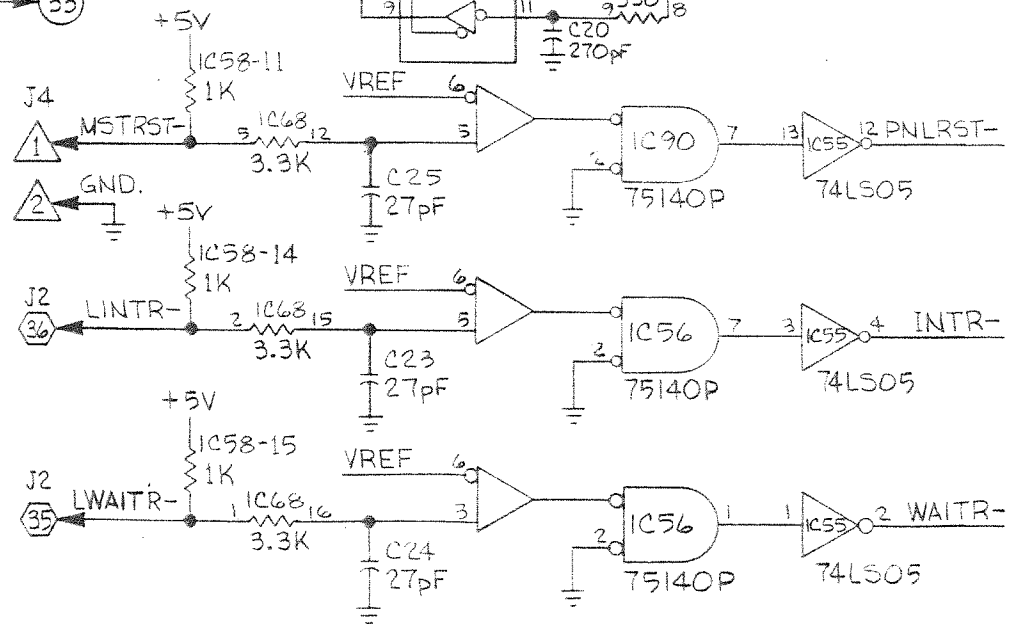
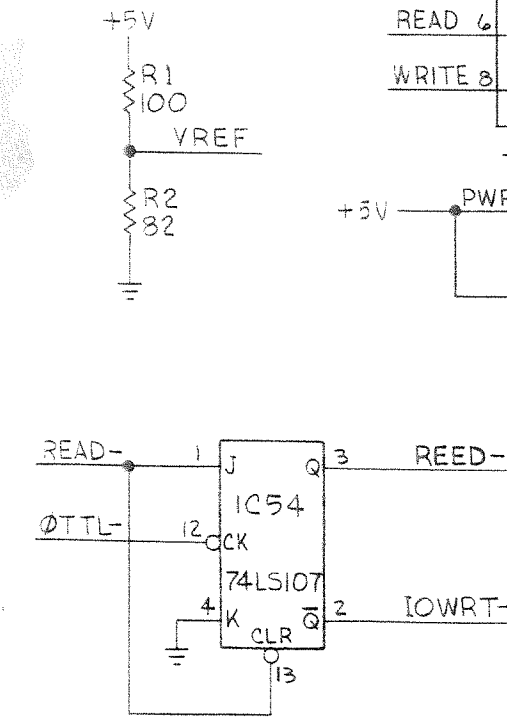
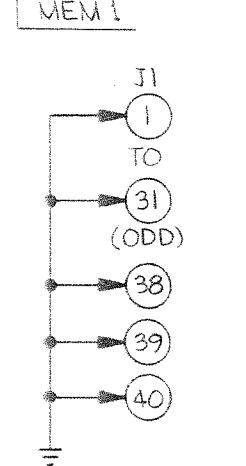
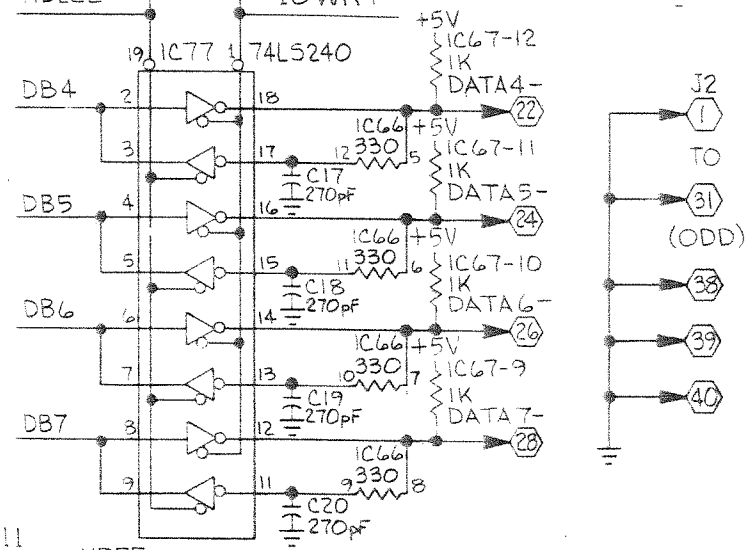
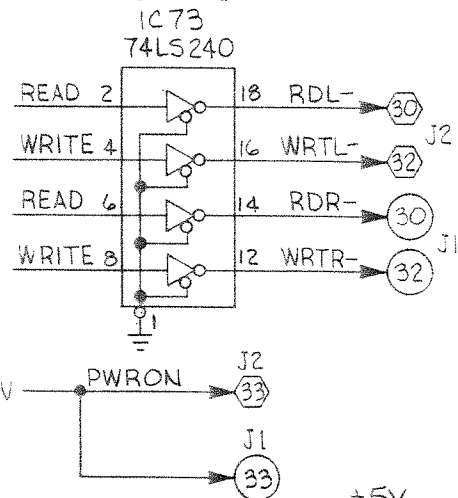
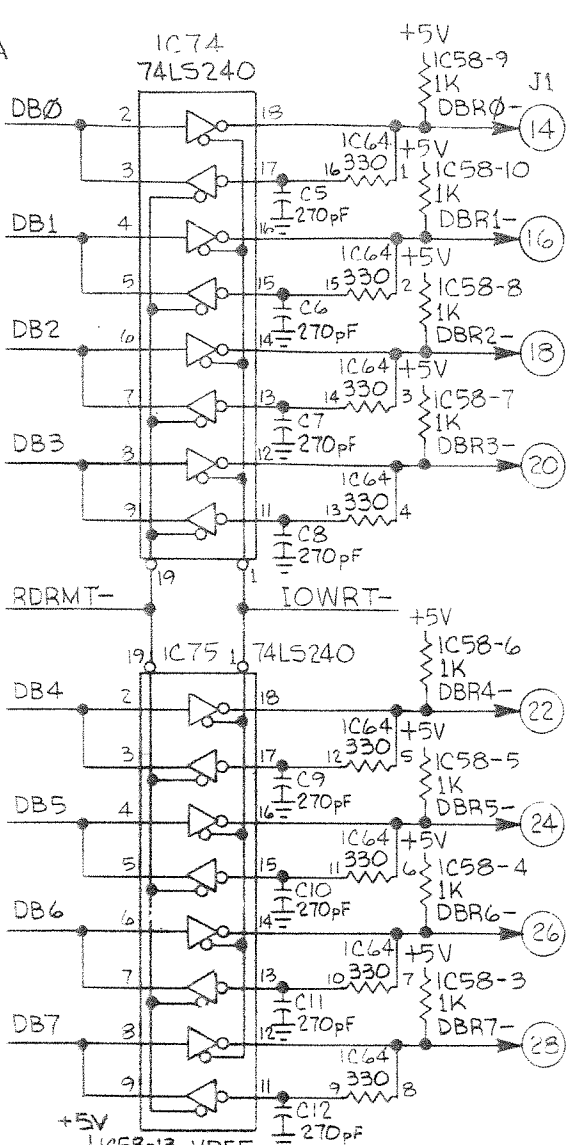
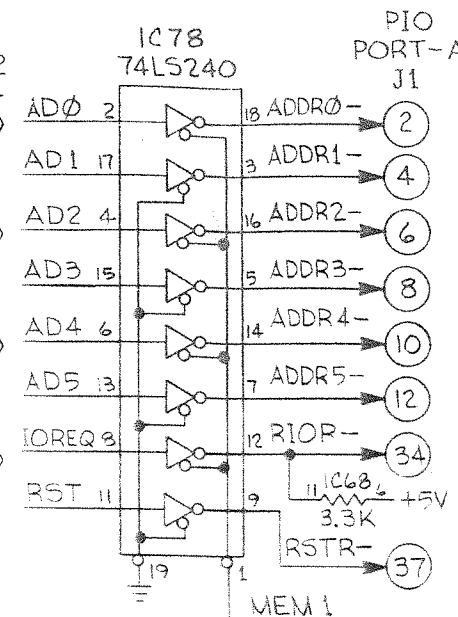
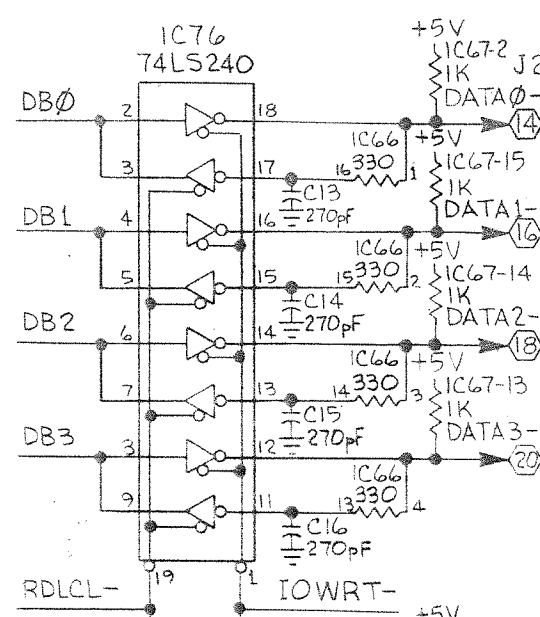
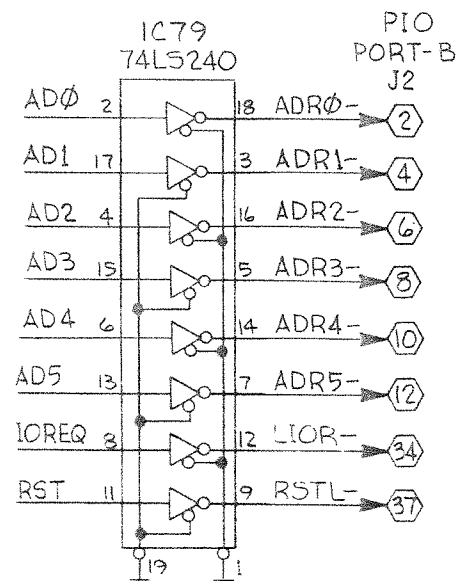


			UNLESS OTHERWISE SPECIFIED		DRAWN BY <u>G. O'GRADY</u> DATE <u>3-24-77</u> TITLE		<div> QI CORPORATION</div> <div>5 Dubon Court Farmingdale, New York 11735</div>					
			ALL DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING		CHKD BY					QI/LITE SYSTEM BOARD RAM LOGIC		
			REMOVE BURRS AND BREAK EDGES .015 MAX		MECH ENGR							
			TOLERANCES ON		ELEC ENGR							
			FRACTIONS DECIMALS ANGLES 1/64 .005 1°		APPROVED							
			NOT APPL TO HOLE DIA.		RELEASE		SEE SEPARATE SHEET FOR LIST OF MATERIALS					
			MATERIAL FINISH				SIZE DWG. NO REV					
DASH NEXT ASSY USED ON							D 007-51004					
APPLICATION							SCALE SHEET 3 OF 11					

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	BY
H		SEE SHT.-1		

TEST PANEL/DMA PORT

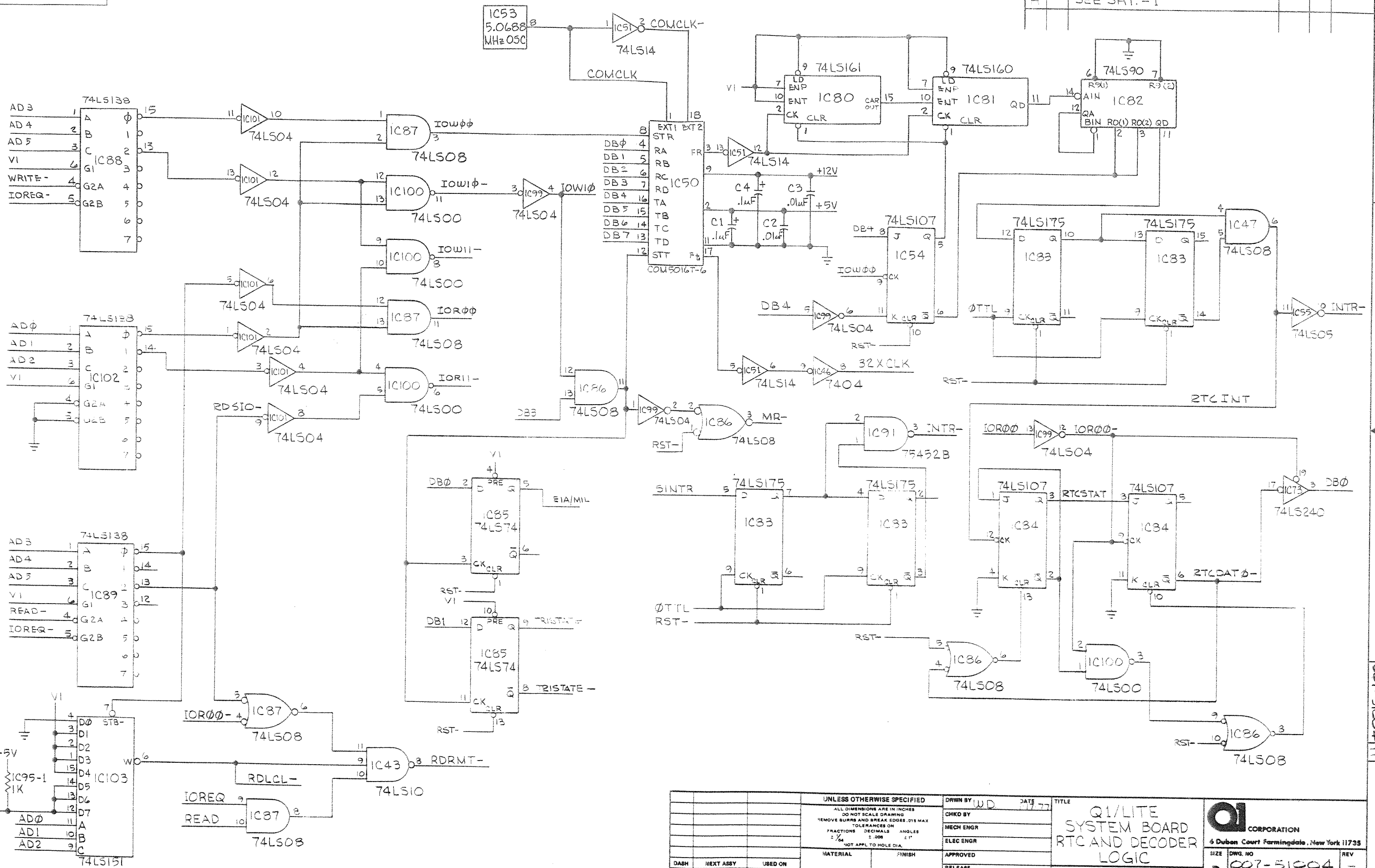
P1		P1	
AD0	40	DB6	30
AD1	38	DB7	76
AD2	36	BUSACK-	96
AD3	54	MEM1-	98
AD4	52	BUSGNT-	94
AD5	50	RST-	92
AD6	48	HALT-	84
AD7	46	IOREQ-	34
AD8	44	MEMREQ-	14
AD9	42	READ-	10
AD10	4	WRITE-	3
AD11	6	REFSH-	18
AD12	2	WAITR-	30
AD13	22	BUSRQ-	32
AD14	20	ADAT-	12
AD15	16	PED-	24
DB0	72	INTR-	26
DB1	64	PNLRST-	28
DB2	74	MREQ-	56
DB3	62	RD-	68
DB4	88	WR-	90
DB5	36	IORQ-	66
		NMI-	78
		INT-	58
		N/C	100
		REFSH-	70
		CTLGNT-	82
		DTTL	60




UNLESS OTHERWISE SPECIFIED			DRAWN BY W.D. DATE 11/22/84		TITLE	
ALL DIMENSIONS ARE IN INCHES			CHKD BY		Q1/LITE	
DO NOT SCALE DRAWING			MECH ENGR		SYSTEM BOARD	
REMOVE BURRS AND BREAK EDGES .015 MAX			ELEC ENGR		PIO	
TOLERANCES ON			APPROVED		LOGIC	
FRACTIONS DECIMALS ANGLES			RELEASE		SEE SEPARATE SHEET FOR	
1/4 2.008 1°					LIST OF MATERIALS	
NOT APPL TO HOLE DIA.						
DASH	NEXT ASSY	USED ON				
APPLICATION						

Q1 CORPORATION	
6 Duban Court Farmingdale, New York 11735	
SIZE	DRG. NO.
D	007-51004
SCALE	SHEET 4 OF 11

REVISIONS					
LTR	ZONE	DESCRIPTION	DATE	BY	APPROVED
1		SEE SHT. - 1			

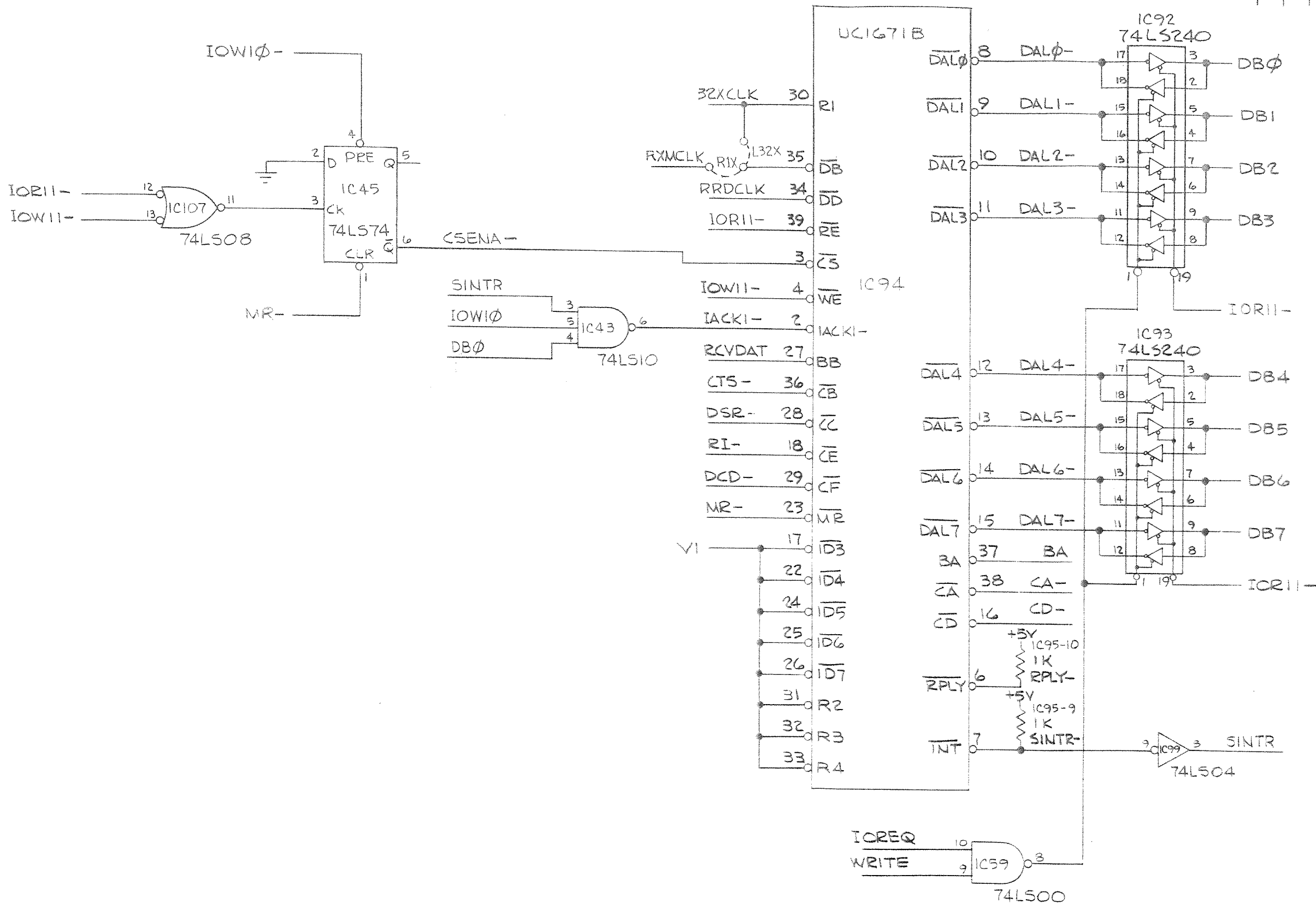


007-51004	11	A
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			UNLESS OTHERWISE SPECIFIED		DRAWN BY <u>WD</u> DATE <u>11-77</u>		TITLE		 QI CORPORATION 6 Dubon Court Farmingdale, New York 11735	
			ALL DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING		CHKD BY		<u>Q1/LITE</u> <u>SYSTEM BOARD</u> <u>RTC AND DECODER</u> <u>LOGIC</u>			
			REMOVE BURRS AND BREAK EDGES .015 MAX TOLERANCES ON		MECH ENGR					
			FRACTIONS DECIMALS ANGLES $\frac{1}{8}$.125 30°		ELEC ENGR					
			NOT APPL TO HOLE DIA.		APPROVED					
			MATERIAL		FINISH		RELEASE		SIZE <u>DWG. NO</u> <u>007-51004</u> REV <u>-</u> SCALE SHEET <u>5</u> OF <u>11</u>	
DASH NEXT ASSY USED ON										
APPLICATION							SEE SEPARATE SHEET FOR LIST OF MATERIALS			

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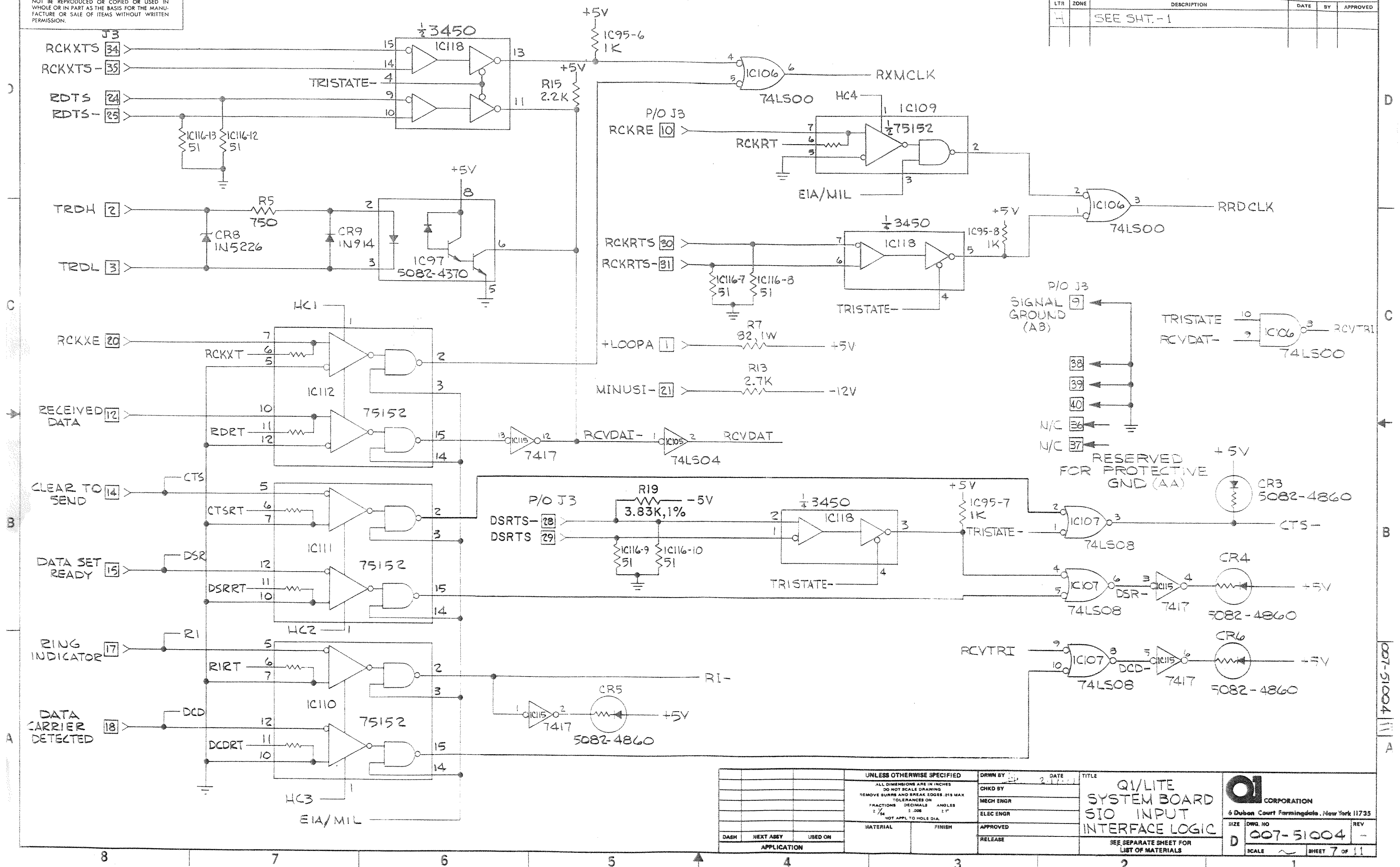
REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	BY
1		SEE SHT. - 1		



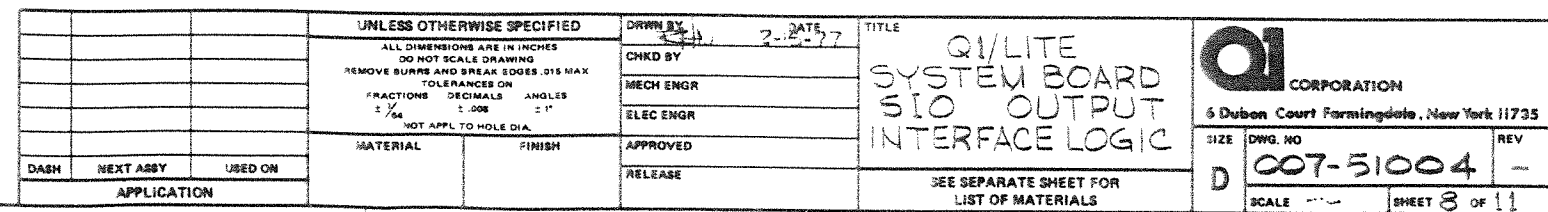
UNLESS OTHERWISE SPECIFIED				DRAWN BY		DATE		TITLE	
ALL DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING REMOVE BURRS AND BREAK EDGES .015 MAX TOLERANCES ON FRACTIONS DECIMALS ANGLES 1/64 1.000 1°				4-11V		2-12-11		Q1/LITE SYSTEM BOARD SIO TRANSCEIVER LOGIC	
MATERIAL				FINISH		APPROVED		Q1 CORPORATION 6 Dubon Court Farmingdale, New York 11735	
DASH				NEXT ASSY		USED ON		SIZE DWG. NO	
APPLICATION				RELEASE		SEE SEPARATE SHEET FOR LIST OF MATERIALS		D 007-51004	
								SCALE ~ SHEET 6 OF 11	

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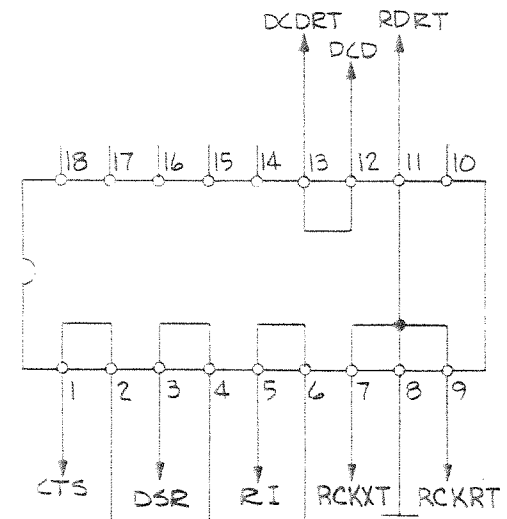
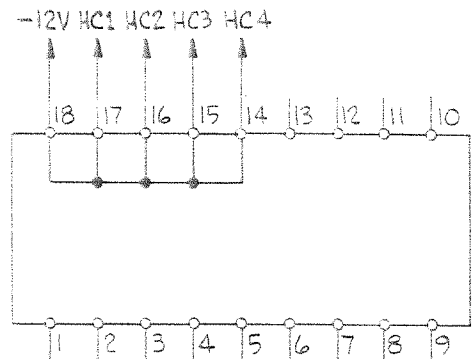
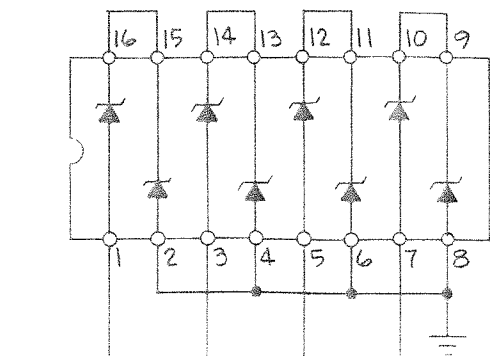
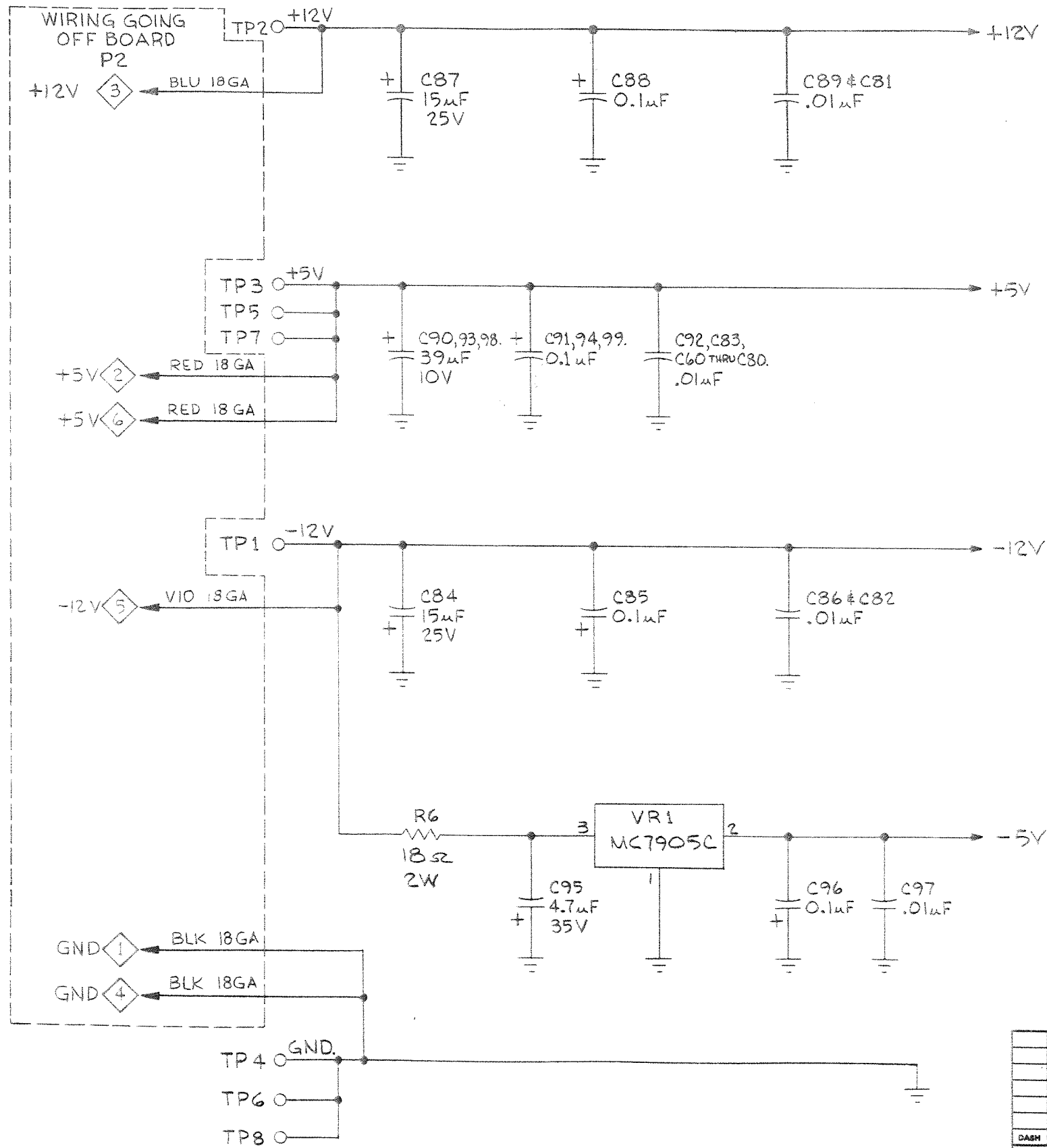
REVISIONS					
LTR	ZONE	DESCRIPTION	DATE	BY	APPROVED
1		SEE SHT. - 1			



REVISIONS					
LTR	ZONE	DESCRIPTION	DATE	BY	APPROVED
H		SEE SHT. - 1			



LTR	ZONE	DESCRIPTION	DATE	BY	APPROVED
4		SEE SHT. - 1			



			UNLESS OTHERWISE SPECIFIED		DRAWN BY <u>2-15-77</u>	DATE <u>2-15-77</u>	TITLE	
			ALL DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING		CHKD BY		Q1/LITE	
			REMOVE BURRS AND BREAK EDGES .015 MAX		MECH ENGR		SYSTEM BOARD	
			TOLERANCES ON		ELEC ENGR		D.C. INPUTS &	
			FRACTIONS DECIMALS ANGLES		APPROVED		HEADER ASSEMBLIES	
			±.04 ±.008 ±.1°		RELEASE		SEE SEPARATE SHEET FOR LIST OF MATERIALS	
			NOT APPL. TO HOLE DIA.					
			MATERIAL		FINISH			
DASH			NEXT ASSY		USED ON			
APPLICATION								
							Q1 CORPORATION	
							6 Duben Court Farmingdale, New York 11735	
					SIZE		DWG. NO	REV
					D		007-51004	-
					SCALE		SHEET 9 OF 11	

REVISIONS				
LTR	ZONE	DESCRIPTION	DATE	BY
1		SEE SHT.-1		

TTL TEST PANEL/DMA PORT				
PI - 40	AD ϕ	I/O	ADDRESS	BUS, CONT/SYS. STAT.
38	AD1			
36	AD2			
54	AD3			
52	AD4			
50	AD5			
48	AD6			
46	AD7			
44	AD8			
42	AD9			
4	AD10			
6	AD11			
2	AD12			
22	AD13			
20	AD14			
16	AD15			
72	DB ϕ		ADDRESS	BUS, CONT/SYS. STAT.
64	DB1		DATA	BUS, CONT/SYS. STAT.
74	DB2			
62	DB3			
38	DB4			
86	DB5			
30	DB6			
76	DB7	I/O	DATA	BUS, CONT/SYS. STAT.
96	BUSACK-	O	CONT.	
98	MEM1-	O	MEM1, CONT/SYS. STAT.	
94	BUSGNT-	O	BUSGNT, FUTURE CONT/SYS. STAT.	
92	RST-	O	RST	
34	HALT-	O	HALT, CPU STAT.	
34	IOREQ-	I/O	IOREQ, CONT/ SYS. STAT.	
14	MEMREQ-I/O		MEMREQ, CONT/ SYS. STAT.	
10	READ-	I/O	READ, CONT/SYS. STAT.	
8	WRITE-	I/O	WRITE, CONT/SYS. STAT.	
18	REFSH-	I/O	REFSH, CONT/SYS. STAT.	
30	WAITR-	I	WAITR, CONT.	
32	BUSRQ-	I	BUSREQ, FUTURE CONT.	
12	ADAT-	I	ADDR, DAT. + CONT.	
24	PED-	I	PED, CONT.	
26	INTR-	I	INTR, CONT.	
28	PNLRST-	I	PNLRST, CONT.	
56	MREQ-	O	MREQ, CPU STAT.	
68	RD-	O	RD, CPU STAT.	
90	WR-	O	WT, CPU STAT.	
66	IORQ-	O	IORQ, CPU STAT.	
78	NMI-	I	NMI, FUTURE CONT.	
58	INT-	O	INT, CPU STAT.	
100	N/C			
70	RFSH-	O	RFSH, CPU STAT.	
82	CTLGNT-	I	CONT.	
PI - 60	ϕ TTL	O	ϕ TTL, CONT.	

1 TO 49 (ODD) GND
51 TO 99 (ODD) +5V

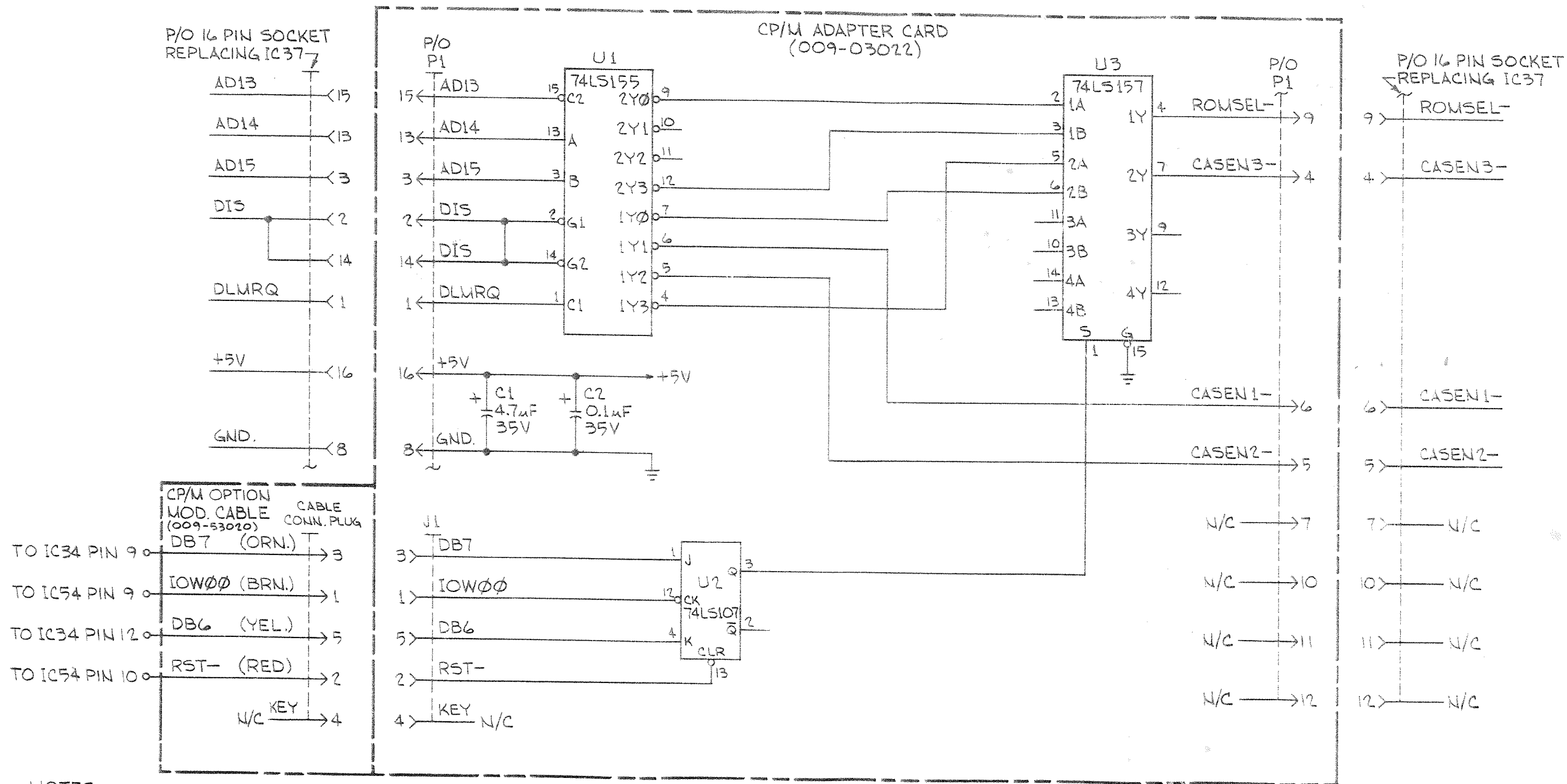
PIO PORT-B				
LCL	TTL	I/O	BUS	
J2 - 1	GND	BRN		
2	ADR ϕ -	RED		
3	GND	ORG		
4	ADR1-	YEL		
5	GND	GRN		
6	ADR2-	BLU		
7	GND	VIO		
8	ADR3-	GRY		
9	GND	WHT		
10	ADR4-	BLK		
11	GND	BRN		
12	ADR5-	RED		
13	GND	ORG		
14	DATA ϕ -	YEL		
15	GND	GRN		
16	DATA1-	BLU		
17	GND	VIO		
18	DATA2-	GRY		
19	GND	WHT		
20	DATA3-	BLK		
21	GND	BRN		
22	DATA4-	RED		
23	GND	ORG		
24	DATA5-	YEL		
25	GND	GRN		
26	DATA6-	BLU		
27	GND	VIO		
28	DATA7-	GRY		
29	GND	WHT		
30	RDL-	BLK		
31	GND	BRN		
32	WRTL-	RED		
33	PWRON	ORN		
34	L1OR-	YEL		
35	LWAITR-	GRN		
36	LINTR-	BLU		
37	RSTL-	VIO		
38	GND	GRY		
39	GND	WHT		
J2-40	GND	BLK		

SIO BUS				
J3 - 1	+LOOPA	BRN		
2	TRDH	RED		
3	TRDL	ORG		
4	TRDLA	YEL		
5	TXDL	GRN		
6	-LOOPA	BLU		
7	+LOOPB	VIO		
8	-LOOPB	GRY		
9	SIG GND (AB)	WHT		
10	RCKRE (DD)	BLK		
11	TRANSMITTED DATA (BA)	BRN		
12	RECEIVED DATA (BB)	RED		
13	REQUEST TO SEND (CA)	ORG		
14	CLEAR TO SEND (CB)	YEL		
15	DATA SET READY (CC)	GRN		
16	DATA TERMINAL READY FLTD (CD)	BLU		
17	RING INDICATOR (CE)	VIO		
18	DATA CARRIER DETECTED (CF)	GRY		
19	ROUT 32XE	WHT		
20	RCKXE (DB)	BLK		
21	MINUSI-	BRN		
22	XMDTS	RED		
23	XMDTS-	ORG		
24	RDTs	YEL		
25	RDTs-	GRN		
26	RTSTS-	BLU		
27	RTSTS	VIO		
28	DSRTS-	GRY		
29	DSRTS	WHT		
30	RCKRTS	BLK		
31	RCKRTS-	BRN		
32	ROUT32XTS	RED		
33	ROUT32XTS-	ORG		
34	RCKXTS	YEL		
35	RCKXTS-	GRN		
36	N/C { PROTECTIVE }	BLU		
37	N/C { GND (AA) }	VIO		
38	GND	GRY		
39	GND	WHT		
J3-40	GND	BLK		

PIO PORT-A				
J1 - 1	RMT TTL	I/O	BUS	
1	GND	BRN		
2	ADDR ϕ -	RED		
3	GND	ORG		
4	ADDR1-	YEL		
5	GND	GRN		
6	ADDR2-	BLU		
7	GND	VIO		
8	ADDR3-	GRY		
9	GND	WHT		
10	ADDR4-	BLK		
11	GND	BRN		
12	ADDR5-	RED		
13	GND	ORG		
14	DBR ϕ -	YEL		
15	GND	GRN		
16	DBR1-	BLU		
17	GND	VIO		
18	DBR2-	GRY		
19	GND	WHT		
20	DBR3-	BLK		
21	GND	BRN		
22	DBR4-	RED		
23	GND	ORG		
24	DBR5-	YEL		
25	GND	GRN		
26	DBR6-	BLU		
27	GND	VIO		
28	DBR7-	GRY		
29	GND	WHT		
30	RDR-	BLK		
31	GND	BRN		
32	WRTR-	RED		
33	PWRON	ORG		
34	RIOR-	YEL		
35	RWAITR-	GRN		
36	RINTR-	BLU		
37	RSTR-	VIO		
38	GND	GRY		
39	GND	WHT		
J1-40	GND	BLK		

UNLESS OTHERWISE SPECIFIED			DRWN BY	DATE	TITLE
ALL DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING REMOVE BURRS AND BREAK EDGES .015 MAX TOLERANCES ON FRACTIONS DECIMALS ANGLES 2/64 2.008 2 1/2			CHKD BY	W.D. 2/16/77	Q1/LITE SYSTEM BOARD I/O CONNECTORS
MATERIAL			APPROVED		Q1 CORPORATION 4 Duben Court Farmingdale, New York 11735
FINISH			RELEASE		SIZE DWG. NO. REV
APPLICATION			SEE SEPARATE SHEET FOR LIST OF MATERIALS		D 007-51004 -
					SCALE SHEET 10 OF 11

REVISIONS			DATE	BY	APPROVED
LTR	ZONE	DESCRIPTION			
1		SEE SHT-1.			



NOTES:

- TO INSTALL THE CP/M OPTION INTO THE SYSTEM BOARD;
A) REMOVE IC37 (SHEET 2) & REPLACE WITH A 16 PIN D.I.P. SOCKET.
B) PLUG CP/M ADAPTER CARD (009-03022) INTO IC37 SOCKET USING P1 ON ADAPTER CARD AS PLUG.
C) PLUG CP/M OPTION MODIFICATION CABLE (009-53020) INTO J1 ON ADAPTER CARD.
D) SOLDER THE (4) WIRES ON THE CABLE TO THE POINTS ON THE SYSTEM BOARD INDICATED ON THE SCHEMATIC ABOVE.

UNLESS OTHERWISE SPECIFIED			DRWN BY	DATE	TITLE
ALL DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWING REMOVE BURRS AND BREAK EDGES .015 MAX TOLERANCES ON FRACTIONS DECIMALS ANGLES			9.0	3-14-80	Q1/LITE SYSTEM BOARD CP/M OPTION
1/4 .005 .010			CHKD BY	MB	2-16-80
MATERIAL			MECH ENGR		
FINISH			ELEC ENGR		
DASH			APPROVED		
NEXT ASSY			RELEASE		
USED ON			SEE SEPARATE SHEET FOR LIST OF MATERIALS		
APPLICATION			SIZE	DWG. NO	REV
			D	007-51004	-
			SCALE	SHEET 11 OF 11	